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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/032,734	12/28/2001	Salman Akram	2754.4US (95-0742.4)	6382

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EXAMINER	
GRAYBILL, DAVID E	
ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 04/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/032,734	AKRAM ET AL.	
	Examiner	Art Unit	
	David E Graybill	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9-22-3 has been entered.

It is noted that the Office action filed on 7-17-3 was directed to the marked-up copy of the claims filed on 11-18-2. However, the marked-up copy of the claims was not identical to the clean copy of the claims concomitantly filed on 11-18-2. For example, the marked-up copy of claim 1 filed on 11-18-2 does not show the deletion of the term "being" and the addition of the terms "wherein" and "has been" as shown on the penultimate line of the clean copy. Additional inconsistencies may have been present. It is further noted that the amendment filed on 9-22-3 appears to be directed to the clean copy of the claims filed on 11-18-2, and not to the marked-up copy which was examined in the Office action filed on 7-17-3.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-4, 6-16, 18 and 34-36 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

There is insufficient antecedent basis for the following:

Claim 1, "said location";

Claims 18 and 35, "the side upon which the second vacant position is located," and, "the side of the substrate which is opposite the side upon which the second vacant position is located."

Claims 16 and 34 are incomplete because they omit essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are those between all of the elements of claims 16 and 34 and the elements of claims 4 and 23, respectively.

In the rejections infra, generally, reference labels are recited only for the first recitation of identical claim elements.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-10, 12, 14, 16-28 and 34-36 are rejected under 35 U.S.C. 102(e) as being anticipated by Lin (6002178).

At column 2, lines 36-41; column 3, lines 18-23 and 33-39; column 3, line 60 to column 5, line 34; and column 7, lines 5-15 and 62-63, Lin discloses the following:

A multi-chip module system comprising: a substrate 110 having at least a first position having, in turn, a configuration 115 and having at least one other vacant position having, in turn, a configuration 115; and a first semiconductor device 120-1 located in the at least first position of the substrate, the first semiconductor device inherently having a first performance characteristic; the at least one other vacant position having the configuration which is substantially the same as the configuration of the first position; the at least one other vacant position having the configuration; a third semiconductor device (lower device illustrated in FIG. 1E, not labeled); and an adapter (element in direct contact with underfill of lower device

illustrated in FIG. 1E, not labeled) connected to the third semiconductor device, the adapter having a configuration.

A multi-chip module system comprising: a substrate having a first position having, in turn, a configuration, having a second position having, in turn, a configuration 115, and having at least one other vacant position having, in turn, a configuration; the first semiconductor device located in the first position of the substrate, the first semiconductor device having a first performance characteristic; and the second semiconductor device 120-2 located in the second position of the substrate, the second semiconductor device inherently having a second performance characteristic.

A multi-chip module system comprising: a substrate having two opposing sides, said substrate having a first position having, in turn, a configuration, having a second position having, in turn, a configuration, having a first vacant position having, in turn, a configuration 115, and having a second vacant position having, in turn, a configuration 115; the first semiconductor device located in the first position of the substrate, the first semiconductor device having a first performance characteristic; and the second semiconductor device located in the second position of the substrate, the second semiconductor device having a second performance characteristic; wherein: the first vacant position is on the side (left side in

FIG. 1D) of the substrate which is opposite the side (right side in FIG. 1D) upon which the second vacant position is located.

A multi-chip module system comprising: a substrate having at least a first configuration 115 position and having at least one other vacant configuration 115 position; and the first semiconductor device located in the at least the first configuration position of the substrate, the first semiconductor device having a first performance characteristic; the at least one other vacant configuration position which is substantially the same as the configuration of the first position; the at least one other vacant configuration position having a configuration.

A multi-chip module system comprising: a substrate having a first configuration position, having a second configuration 115 position, and having at least one other vacant configuration position; the first semiconductor device located in the first configuration position of the substrate, the first semiconductor device having a first performance characteristic; and the second semiconductor device located in the second configuration position of the substrate, the second semiconductor device having a second performance characteristic; the at least one other vacant configuration position which is substantially the same as the configuration of the first position; an adapter connected to the third semiconductor device.

A multi-chip module system comprising: a substrate having two opposing sides (left and right sides in FIG. 1D), said substrate having a first configuration position, having a second configuration position, having a first vacant configuration position, and having a second vacant configuration; the first semiconductor device located in the first configuration position of the substrate, the first semiconductor device having a first performance characteristic; and the second semiconductor device located in the second configuration position of the substrate, the second semiconductor device having a second performance characteristic; the first vacant configuration position is located on the side of the substrate which is opposite the side upon which the second vacant configuration position is located.

Also, as cited, Lin explicitly discloses the following process limitations:

Wherein said first semiconductor device has been burned in at said location on said substrate; said first and second semiconductor devices have been burned in at said first and second positions, respectively, on said substrate; said first and second semiconductor devices being burned in at said first and second positions, respectively, on said substrate; said first semiconductor device being burned in at said first configuration position on said substrate; wherein said first and second semiconductor devices being burned in at said first and second configuration positions, respectively, on said substrate; said first and second semiconductor devices have been

burned in at said first and second configuration positions, respectively, on said substrate.

Although Lin does not appear to explicitly disclose the process limitations "predetermined," both the configurations and the performance characteristics (KGD or KBD) are determined in advance of any subsequent event; hence, they are inherently predetermined.

In any case, notwithstanding the explicit and inherent disclosures of these process limitations, the product of Lin inherently possesses any structural characteristics imparted by the process limitations. See In re Fitzgerald, Sanders, and Bagheri, 205 USPQ 594 (CCPA 1980).

The following claim limitations are statements of intended use:

For locating a first semiconductor device thereat; for locating a second semiconductor device thereat on the multi-chip module system; for use in the multi-chip module system; for locating the second semiconductor device thereat; for locating the second semiconductor device thereat, and the second semiconductor device having a predetermined performance characteristic substantially similar to that of the first predetermined performance characteristic of the first semiconductor device; for locating the second semiconductor device thereat, and the second semiconductor device having a second predetermined performance characteristic of at least substantially twice that of the first predetermined performance characteristic

of the first semiconductor device; for locating a first semiconductor device thereat; for locating a second semiconductor device thereat; for locating a third semiconductor device thereat on the multi-chip module system; for use in the multi-chip module system; for use in the multi-chip module system; for locating a third semiconductor device thereat; for locating a third semiconductor device thereat, and the third semiconductor device having a predetermined performance characteristic substantially similar to that of the first predetermined performance characteristic of the first semiconductor device; for locating a third semiconductor device thereat, and the third semiconductor device having a predetermined performance characteristic of at least substantially twice that of the first predetermined performance characteristic of the first semiconductor device; for locating a third semiconductor device thereat, and the third semiconductor device having a predetermined performance characteristic of at least substantially three times greater than that of the second predetermined performance characteristic of the second semiconductor device; for locating a third semiconductor device thereat, and the third semiconductor device having a predetermined performance characteristic of at least substantially four times greater than that of the first and the second predetermined performance characteristic of the first semiconductor device and the second semiconductor device combined; wherein the second semiconductor device

comprises a memory device; wherein the second semiconductor device comprises a microprocessor device; for connecting the adapter to the at least one other vacant position on the substrate to connect the third semiconductor device to the substrate; for locating a first semiconductor device thereat; for locating a second semiconductor device thereat; for locating a third semiconductor device thereat; for locating a fourth semiconductor device thereat on the multi-chip module system; for use in the multi-chip module system; for use in the multi-chip module system; for locating a first semiconductor device thereat; for locating a second semiconductor device thereat on the multi-chip module system; for use in the multi-chip module system; for locating the second semiconductor device thereat; for locating the second semiconductor device thereat, and the second semiconductor device having a predetermined performance characteristic substantially similar to that of the first predetermined performance characteristic of the first semiconductor device, for locating the second semiconductor device thereat, and the second semiconductor device having a predetermined performance characteristic of at least substantially twice that of the first predetermined performance characteristic of the first semiconductor device; for locating a first semiconductor device thereat; for locating a second semiconductor device thereat; for locating a third semiconductor device thereat on the multi-chip module system; for use in

the multi-chip module system; for use in the multi-chip module system; for locating the third semiconductor device thereat; for locating the third semiconductor device thereat, and the third semiconductor device having a third predetermined performance characteristic substantially similar to that of the first predetermined performance characteristic of the first semiconductor device; for locating the third semiconductor device thereat, and the third semiconductor device having a third performance characteristic of at least substantially twice that of the first performance characteristic of the first semiconductor device; for locating the third semiconductor device thereat, and the third semiconductor device having a third predetermined performance characteristic of at least substantially three times greater than that of the second predetermined performance characteristic of the second semiconductor device; for locating a third semiconductor device thereat, and the third semiconductor device having a third predetermined performance characteristic of at least substantially four times greater than that of the first and second predetermined performance characteristic of the first semiconductor device and the second semiconductor device combined; the adapter for connecting the adapter to the at least one other vacant predetermined configuration position on the substrate to connect the third semiconductor device to the substrate; for locating a first semiconductor device thereat; for locating a second semiconductor device thereat; for

locating a third semiconductor device thereat; for locating a fourth semiconductor device thereat on the multi-chip module system; for use in the multi-chip module system; for use in the multi-chip module system.

Although Lin discloses many of these intended use limitations, Lin does not appear to explicitly disclose all of them.

Nonetheless, none of these statements of intended use of the multi-chip module result in a structural difference between the claimed multi-chip module and the multi-chip module of Lin. For example, in claim 3, the intended use limitation, "for locating the second semiconductor device thereat," does not structurally limit the claimed multi-chip module to a second semiconductor device located thereat; hence, the limitation of the absent second semiconductor device structure, "and the second semiconductor device having a predetermined performance characteristic substantially similar to that of the first predetermined performance characteristic of the first semiconductor device," does not further limit the scope of the claims.

Further, because the multi-chip module of Lin has the same structure as the claimed multi-chip module, it is inherently capable of being used for the intended uses, both those intended uses explicitly and not explicitly disclosed, and the statements of intended use do not patentably distinguish the claimed multi-chip module from the multi-chip module of Lin. The

manner in which a product operates is not germane to the issue of patentability of the product; Ex parte Wikdahl 10 USPQ 2d 1546, 1548 (BPAI 1989); Ex parte McCullough 7 USPQ 2d 1889, 1891 (BPAI 1988); In re Finsterwalder 168 USPQ 530 (CCPA 1971); In re Casey 152 USPQ 235, 238 (CCPA 1967). Also, "Expressions relating the apparatus to contents thereof during an intended operation are of no significance in determining patentability of the apparatus claim."; Ex parte Thibault, 164 USPQ 666, 667 (Bd. App. 1969). And, "Inclusion of material or article worked upon by a structure being claimed does not impart patentability to the claims."; In re Young, 25 USPQ 69 (CCPA 1935) (as restated in In re Otto, 136 USPQ 458, 459 (CCPA 1963)). And, claims directed to product must be distinguished from the prior art in terms of structure rather than function. In re Danley, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does [or is intended to do]." Hewlett-Packard Co. v. Bausch & Lomb Inc., 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

Claims 11, 15, 29, 30 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (6002178).

Lin is applied for the same reasons it was applied to claims 4 and 24.

However, Lin does not appear to explicitly disclose wherein the first semiconductor device comprises a memory device; wherein the multi-chip module system comprises a single in-line memory module system; wherein

the second semiconductor device comprises a memory device; and wherein the multi-chip module system comprises a single in-line memory module system.

Still, as cited supra, Lin discloses that the "MCM board can be used for different kinds of integrated circuit chips," and, "can be broadly applied to assemble various kind of electronic packages." And, at column 1, lines 16-29, Lin discloses as conventional wherein the first semiconductor device comprises a memory device; wherein the multi-chip module system comprises a single in-line memory module system; wherein the second semiconductor device comprises a memory device; and wherein the multi-chip module system comprises a single in-line memory module system. Moreover, it would have been obvious to use the conventional devices as the devices of Lin because it would provide the MCM of Lin, and use of a known element based on its suitability for its intended use has been held to be prima facie obvious. See MPEP 2144.07.

Claims 13, 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin as applied to claims 4 and 23, and further in combination with Falcone (5836071).

Lin does not appear to explicitly disclose wherein the first semiconductor device comprises a microprocessor device; and wherein the second semiconductor device comprises a microprocessor device.

Regardless, at column 1, lines 14-19, Falcone discloses wherein MCMs comprise microprocessor devices. In addition, it would have been obvious to combine the microprocessor device of Falcone with the MCM of Lin because it would enable creation of high performance products.

Applicant's amendment and remarks filed 9-22-3 have been fully considered and are adequately addressed by the new grounds of rejection supra.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to Group 2800 Customer Service whose telephone number is 571-272-2815.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is (703) 872-9306.

David E. Graybill
Primary Examiner
Art Unit 2827

D.G.
1-Apr-04